IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	
	)	
OOSAWA et al.	)	
	)	
Serial Number: 10/615,787	)	**Art Unit 2829**
	)	
Filed: July 10, 2003	)	**Examiner Jimmy Nguyen**
	)	
For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE	)	
	)	
Attorney Docket No. HITA.0413	)	

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

TERMINAL DISCLAIMER

Sir:

We, Stanley P. Fisher and Juan Carlos A. Marquez, represent that we are the attorneys of record for the above-identified application.

The invention has been assigned to Hitachi, Ltd., who is the owner by assignment of the entire right and title of the above-captioned patent application.

Hitachi, Ltd. is also the owner of the entire right and title to US Patent No. 6,597,191 by assignment, and hereby disclaims the terminal part of any patent granted on the above-captioned patent application, which would extend beyond the expiration date of the full statutory term as presently shortened by any terminal disclaimer of U.S. Patent No. 6,597,191, and hereby agrees that any patent so granted on the above-captioned application shall be enforceable only for and during such period that the legal title to said patent shall be the same as the legal title to U.S. Patent No. 6,597,191, this agreement to run with any patent granted on the above-captioned application and to be binding upon the grantee, its successors or assigns.

No rights available under the provisions of 35 U.S.C. § 155 and 156 are hereby waived.

Petitioner does not disclaim any terminal part of any patent granted on the above-captioned application prior to the expiration date of the full statutory term as presently shortened by any terminal disclaimer of US Patent No. 6,597,191, in the event that it later expires for failure to pay a maintenance fee, is held unenforceable, if found invalid, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. § 1.321(a), has all claims cancelled by a reexamination certificate, or is otherwise terminated prior to the expiration of its statutory term as presently shortened by any terminal disclaimer, except for the separation of legal title stated above.

Respectfully submitted,

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Substitute Abstract of the Disclosure

An input/output pin for testing corresponding to a test circuit of the digital section is used in common as the input/output pin for normal operation of the analog section. The selection switches are respectively provided between the relevant analog pin and analog circuit and on a signal line up to the test circuit of the digital section from the relevant analog pin and the switches are provided at both end portions of the signal line between the test circuit of digital section and the input/output pin for common use in order to fix the voltage of the signal line to the predetermined voltage such as the ground voltage during the normal operation. Thereby, it is possible in a semiconductor integrated circuit having the analog and digital sections to eliminate any adverse effect, even if the input/output pin for testing corresponding to the test circuit of the digital section is used in common as the input/output pin for normal operation of the analog section, from the analog circuit due to the noise which is generated in the digital section and is then transferred to the analog circuit through the signal path up to the analog input/output pin connected to the test circuit from this test circuit of the digital section.